Optimisation of Boron Predeposition for etch stop

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Abstract
This report was written to document the work carried out and the results obtained in the project titled “Optimisation of Boron Predeposition for etch stop” during the 3-week course. In the lab boron was diffused into Silicon by transferring it from boron nitride wafers onto silicon wafers at high temperature. Over a certain threshold, boron doped silicon is not affected considerably by KOH etching while the undoped silicon is etched away. This is used to make structures that are used in some MEMS applications. Manufacturing these structures requires proper control over the concentration of Boron in the surface of the wafer. A phaselayer of silicon and boron must be removed by oxidation but this also removes boron from the silicon. In a previously used process the boron was too low leaving a very rough surface after etching. This project was about how to control the removal of the phaselayer while maintaining a desired concentration of Boron in silicon. In the frame of the project the program SUPREM by Silvaco is used to examine diffusion and the possibility to predict the processes used in the lab.

Figure 1. SEM picture of structure.
Experimental work
There are four basic operations during processing of semiconductor devices

- Layering
- Patterning
- Doping
- Heat treatment

The processes that were done during this course are presented below together with a description of the tools used, the problems, some theory and the safety issues involved. For an overview of the Process-flow see appendix A.

1.) Oxidation of the wafer

2.) Resist layer is added

3.) Photolithography

4.) Development

5.) Oxide etch

6.) Strip resist

7.) Boron predep with boronglass

8.) Etch until boronglass has gone

9.) Etch of oxide layer

10.) KOH etch

Figure 2. Process flow.
Step 1, Preparation of wafers

We used 15 wafers of type ON70
- One side is polished
- Resistivity: 1-20Ωcm (3e16 phosphorus)
- n-type
- Orientation: <100>
- Thickness: 525±25μm

Method
- The wafers are thermally oxidized with program wet 1000
- After this the thickness of the oxide layer on the wafers is measured with ellipsometry.

Thermal Oxidation
The most common method for the oxidation process is thermal oxidation because it provides the highest quality oxide with lowest interface trap densities. Interface traps result because the crystal structure is non-uniform at the surface and chemical bonding is not necessarily identical to the one underneath the surface. This is a consequence of a discontinuity in the crystal structure of the wafer. The more the interface trap density, the poorer are the dielectric properties of an oxide layer. It is so because the there is always a likelihood that these traps will capture electrons from the neighbourhood due to which the layer will not be a perfect insulator. In thermal oxidation, silicon is subjected to heating in a furnace at elevated temperatures in the presence of a gas containing O₂ or H₂O. Depending on whether O₂ or H₂O is used, the process is termed dry or wet oxidation respectively with wet oxide having four times faster growth rate than the dry oxide due to the smaller size of the H₂O molecule compared to the O₂ molecule. Wet oxidation results in 5-10 times thicker oxide compared to the dry oxidation at the same temperature and pressure. Dry oxide, though slower to grow, is denser and has better dielectric strength. Oxidation is a self-limiting process, in that as the oxidation grows, it eventually prevents the oxygen from reacting with the silicon. Oxidation of Silicon is very important for two reasons:
- It acts as an implantation mask.
- It serves as a protective layer for the semiconductor devices.

The thermal oxidation process is governed by the following chemical reactions:

dry oxidation: \( Si + O_2 \rightarrow SiO_2 \)
wet oxidation: \( Si + 2H_2O \rightarrow SiO_2 + 2H_2 \)
Growth of an oxide layer consumes the underlying silicon from the surface of the wafer. Growing an oxide of thickness \( x \) consumes a layer of silicon \( 0.44x \). The thickness of the oxide needed for diffusion masking is a function of the type of diffusant in addition to the diffusion time and temperature. Generally an oxide layer of 5000Å is sufficient to mask against all diffusions and high energy implantations.

![Figure 3, Oxidation](image)

**Ellipsometry**

Ellipsometry is a technique that can be used for the measurement of the thickness of thin films. The thickness of the film should be less than the wavelength of the incident light for ellipsometry to work. The ellipsometer's name is derived from the elliptical polarization of the light used to measure the thickness and index of refraction of transparent films. The system detects the change in the polarization-state of the light, which occurs when the light is reflected from the surface of the sample, and then calculates the thickness and index of the film based on this change. The components on the polarizer arm produce the elliptically polarized light. The polarizer arm orients the incident light beam at an angle of 70 degrees with respect to the normal of the sample wafer that has been placed upon the wafer stage. The reflected beam is examined by the analyser arm components, which are also oriented at the same fixed angle with respect to the wafer. By rotating the polarizer to a critical angle, and thus preparing a unique polarization state of the incident light, the reflected beam will be linearly polarized. If the analyser is now rotated at 90 degrees to this line of polarization, the intensity of the light passing through the analyser and striking the photo multiplier tube will be a minimum, ideally zero.
The instrument is "tuned" to this null (automatically), and the values of the polarizing filter angle and the analysing filter angle are used by the system to calculate the thickness (t) and index of refraction (n) of the film. Since several values of thickness will produce the same analyser and polarize settings for the null, unique thickness is not determined. You must have a rough estimate of the thickness, and then select that value of thickness calculated by the system, which most closely matches your estimate. The ellipsometer will then provide a very accurate measurement of the film's thickness.

The thickness of oxide layer on our test wafers measured with the Ellipsometer: 5690Å≈600µm

**Step2, Photolithography**

**Method**
1.) HMDS prime of wafers to make the resist stick better to the wafers.
2.) Resist is added on the front side. In the automated process the wafers are prebaked to stabilize the resist.
3.) Exposure: We use a positive process. Exposure time is 16sec.
4.) Development: 45sec. in NaOH (Az3513)
5.) Hardbaking in oven 120°C for 25min. to ensure hardening of resist.
6.) The asher is used to strip any residual resist from the pattern – meaning low power. Power is set to 170W, O₂ 120ml/min. N₂ 20ml/min. time is 2min.

Photolithography is the process by which microscopically small circuits and device patterns can be produced on silicon wafers. A typical photolithography process is composed of the following seven steps.

1. Photoresist Application
A drop of light sensitive liquid is applied to the centre of a silicon wafer that is then spun at 3000-7000 revolutions per minute for about 30-60 seconds. This creates a layer of photo resist about 5,000-10,000Å thick. The thickness of the layer is inversely proportional to the square root of the rotational velocity. Sometimes before application of the photoresist, the wafer is heated to 100°C to get rid of moisture and to obtain better adhesion.

2. Prebake
The wafers are then put into an oven and heated up to 80°C for about 30-60 minutes to drive off solvents and harden it into a semi-solid film.

3. Alignment
When working with dimensions in microns, proper alignment becomes crucial for successful manufacturing of semiconductor devices. To achieve this, the
wafer is placed in an apparatus called a mask aligner at a very close distance to a glass plate called a photo mask. Once properly aligned, the photo mask is brought into contact with the wafer. This method is called contact printing and is used in our case for its precise masking, though other methods exist.

4. Development
The wafer is then exposed to ultraviolet light and then developed. Development can be of two types depending on whether a positive or negative photoresist is used. In case of a negative photoresist, the area exposed to the UV light hardens and becomes insoluble in developer solution. Consequently, unexposed area is dissolved and removed. In case of a positive photoresist, the exposed area depolymerizes and becomes readily soluble in developer solution. This results in the exposed area being dissolved and removed.

5. Postbake
The wafer is kept in an oven at 120°C -150°C for 30-60 minutes to toughen up the remaining photoresist for the following reasons: 1) to make it adhere better and 2) to make it more resistant to the HF solution that is used as an oxide etchant in the following step.

6. Oxide Etching
There are two popular methods for etching
a) Wet Etch: The wafer is immersed in a 10:1 HF solution. The etching rate is 1000Å/s at 25°C. It’s an isotropic etching so etching time must be observed carefully to avoid “undercutting.” The underlying silicon remains unaffected.

b) Dry Etch (plasma etching): CF₄ (Feron14) or C₂H₆ are broken into highly reactive radicals that react with the SiO₂ to form various Si compounds and O₂. The underlying silicon is not overly affected. The advantage of this method is finer line width is obtained in comparison to a wet etch.

7. Stripping Off Photoresist
It’s easier to remove positive photoresist by using an organic solvent like acetone. However, the negative photoresist is harder to remove, as mechanical scrubbing may be needed in addition to hot sulphuric acid. A plasma asher system can be used to remove residual photoresist.
How we did it in the lab
HMDS (Hexamethyldisilazane)
Hexamethyldisilazane (HMDS) is widely used in the semiconductor industry to improve photoresist adhesion to oxides. The HMDS reacts with the oxide surface in a process known as silylation, forming a strong bond to the surface. The methyls, meanwhile, will bond with the photoresist, enhancing the photoresist adhesion.

SAFETY
It should be noted that HMDS is a suspected carcinogen, so it should be handled with care. Do not allow it to contact your skin and avoid inhalation. Always use appropriate boat handling apparatus. Do not place a hot cassette on plastic surfaces or clean room wipes.

PHOTORESIST
Photoresist is a light sensitive layer, which is deposited onto the wafer and exposed to high intensity ultra violet light through a mask. The exposed photoresist is dissolved with a developer solution in positive photolithography, leaving a pattern of photoresist, which allows etching to take place in the exposed areas while unexposed areas stay unaffected. We used a positive photolithography process whereas in negative photolithography unexposed areas of resist can be removed and the exposed areas stay unaffected.

For Integrated circuits the typical thickness after baking ranges between 0.5 to 2 micrometer and for micro fabricated structure thickness from 1µm and above.

Residual removal of PR is made by means of plasma Asher. Usually we go through the rough and fine strip by dipping the wafers into acetone and then into ultrasonic cleaner before going to the plasma asher to remove the leftover photoresist.

Plasma Asher
The Plasma Asher system is used for ashing of photoresist. In plasma ashing, a radio frequency (RF) electric field breaks down the non-reactive gaseous $O_2$ molecules into plasma of reactive mono-atomic oxygen radicals. The highly reactive radicals react with the organic polymers in the photoresist to form gaseous products (CO, CO$_2$, gaseous H$_2$O, etc.) that are pumped away.

Step3, SiO$_2$ etch
Method
- SiO$_2$ etch in BHF (Buffered HF with high etch-rate) to define mask for Boron dep.
- After etching for 10min. the wafers are rinsed in DI-water in two steps for 5min. etch rate 75nm/min
BHF (Buffered Hydro Fluoric Acid)
Hydro Fluoric acid, an acid used to etch silicon dioxide, is often diluted or buffered (a constant PH) when it is used. A mix of hydrogen fluoride and ammonium fluoride ($\text{NH}_4\text{F}$) is used to allow oxide etching at slow controlled rates.

SAFETY
HF acid is very dangerous, HF burns are particularly hazardous. An insidious aspect of HF burns is that there may not be any discomfort until long after exposure. These burns are extremely serious and may result in severe tissue damage. If you get in contact with HF, flush the area well and be sure to work under and around your fingernails. Fingernails are the classic areas where people receive burns, having washed off the HF without washing under their nails. If washed off within a few minutes of exposure, HF may do no harm. HF may not produce any burning sensation until after it has already done damage. A physician should look at all HF burns. Call for help to the person nearest you and while you are speaking to the person nearest you, get to the nearest shower or eyewash as fast as possible.
Exposure of the eyes requires flushing with water for at least 15 minutes.
Exposure of the skin requires immediate removal of all contaminated clothing. Rinse under the shower for 15 minutes and continue rinsing.

Step 4 Strip resist and RCA-clean
Contaminants present on the surface of silicon wafers at the start of processing, or accumulated during processing, have to be removed at specific processing steps in order to obtain high performance and high reliability semiconductor devices, and to prevent contamination of process equipment, especially the high temperature oxidation, diffusion, and deposition tubes. In 1970, the RCA Laboratories developed a cleaning procedure for silicon semiconductor device fabrication technology, which has become the industry standard; it uses several reagents containing hydrogen peroxide.

The RCA cleaning procedure has two major steps used sequentially
- Removal of insoluble organic contaminants with a 5:1:1 $\text{H}_2\text{O} + \text{H}_2\text{O}_2 + \text{NH}_4\text{OH}$ solution (RCA -1).
- Removal of ionic and heavy metal atomic contaminants using solution of 6:1:1 $\text{H}_2\text{O} + \text{H}_2\text{O}_2 + \text{HCL}$ (RCA-2).

The RCA cleaning technique does not attack silicon, and only a very thin layer of silicon dioxide is removed in the process.
Method

Stripping of resist:
1.) 8min in 5% HF + 2min. in DI-water + 3min. in bubbler (N$_2$)
2.) The resist is stripped in acetone for 1min. in prebath
3.) Another 5min. in clean acetonebath.
4.) After this the wafers are rinsed in DI-water in two steps for 3min.

RCA-clean:
This step assures that the wafers are chemically clean. This is important for not to contaminate the ovens. The RCA-clean consists of:
1.) H$_2$O$_2$ + NH$_4$OH + H$_2$O, 10min. 70°C
2.) H$_2$O rinse for 1min.
3.) H$_2$O + N$_2$ bubbles rinse for 2min.
4.) HF, 30sec.
5.) H$_2$O + N$_2$ bubbles rinse for 2min.
6.) H$_2$O$_2$ + HCL + H2O, 10 min. 70°C
7.) H$_2$O rinse for 1min.
8.) H$_2$O + N$_2$ bubbles rinse for 2min.
9.) HF, 30sec.
10.) H$_2$O + N$_2$ bubbles rinse for 5min

SAFETY
The chemicals used for RCA cleaning are all dangerous if you get in contact with them. Acid protective gear MUST be worn when working at the fume hood for RCA. Acid-proof gloves atop the normal clean room gloves, and an acid facemask with the face shield MUST be worn. Exposure of the eyes to any chemical requires immediate excessive flushing of eyes with water for at least 15 minutes.
Step 5. Boron predeposition
Now boron is deposited on the surface using an oven and boron wafers. In the area next to the wafers, around $1 \times 10^{20}$ atoms/cm$^3$ of boron is present. Heating and cooling is done at $10^\circ$/min.

The old process:
Boron predeposition with oxidation

<table>
<thead>
<tr>
<th>Temperature</th>
<th>1125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heating</td>
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<tr>
<td>$\text{N}_2$-flow [Std L pr.min.]</td>
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</tr>
<tr>
<td>$\text{O}_2$-flow [Std L pr.min.]</td>
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<tr>
<td>Time at maxtemp. [min]</td>
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</tr>
<tr>
<td>$\text{N}_2$-flow [Std L pr.min.]</td>
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</tr>
<tr>
<td>$\text{O}_2$-flow [Std L pr.min.]</td>
<td>0.2</td>
</tr>
<tr>
<td>Cooling</td>
<td></td>
</tr>
<tr>
<td>$\text{N}_2$-flow [Std L pr.min.]</td>
<td>3</td>
</tr>
<tr>
<td>$\text{O}_2$-flow [Std L pr.min.]</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 1, Old process

This has some severe disadvantages concerning the ability to control the boron drive in as it is done in the same step as the predeposition. Therefore we will try to separate the processes in two to gain more control over the process. This is done to make the distance with insufficient boron content smaller to gain better surface properties. The surface of the wafers are insufficiently rough with this old process.

![Figure 4, Etchstop](image)
The new process:
Boron predeposition

<table>
<thead>
<tr>
<th>Temperature</th>
<th>1125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heating</td>
<td></td>
</tr>
<tr>
<td>N₂-flow [Std L pr.min.]</td>
<td>2</td>
</tr>
<tr>
<td>O₂-flow [Std L pr.min.]</td>
<td>0</td>
</tr>
<tr>
<td>Time at maxtemp. [min]</td>
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</tr>
<tr>
<td>N₂-flow [Std L pr.min.]</td>
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</tr>
<tr>
<td>O₂-flow [Std L pr.min.]</td>
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<tr>
<td>Cooling</td>
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</tr>
<tr>
<td>N₂-flow [Std L pr.min.]</td>
<td>2</td>
</tr>
<tr>
<td>O₂-flow [Std L pr.min.]</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 2, New Process

0.2 Std L pr.min. of O₂ is used in the predeposition to assist the boron flow into the wafers.

Oxidation step.
In this step the samples are heated in a more controlled way to ensure better final properties. The smaller temperatures make it harder for the impurities to move meaning that the boron profile will rise steeper at the surface. This should possibly give a better surface roughness.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>750°C</th>
<th>800°C</th>
<th>1000°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>H₂-flow [Std L pr.min.]</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>O₂-flow [Std L pr.min.]</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Time at maxtemp. [min]</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>H₂-flow [Std L pr.min.]</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>O₂-flow [Std L pr.min.]</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>N₂-flow [Std L pr.min.]</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 3, Oxidation

Step 6, Stripping oxide
Oxide is stripped in buffered HF to remove the phaselayer obtained in step 5. After dipping in H₂O for 2min. we test every 2 min. whether the wafers are hydrophobic to see if the phaselayer is removed. The phaselayer is hydrophilic and pure Si is hydrophobic. After around 12 min. most of the wafers were hydrophobic.
Step 7. Profile and resistivity measurement

SIMS (Secondary ion mass spectrometer)

We use the SIMS to measure the profile of boron and phosphorus in the test-wafers. As only small specimens can be put into the SIMS we break the wafer in pieces. In the SIMS the test specimens are bombarded with oxygen ions to sputter a certain area on the target. In our case the ion beam scanned a rectangular area. Some of the atoms removed from the surface of the test specimen are exited to a state and secondary ions are then measured in a mass spectrometer attached to the SIMS. Positive or negative ions can then be mass-separated and detected by an electron multiplier or projected onto a screen in order to measure their spatial distribution on the surface. As only the mass will be measured, some measurement inaccuracy will be present, as other particles with the same mass will also come in the test.

Monitoring the intensity of secondary ions as a function of time provides a profile of elemental concentration (providing standards are available) as a function of depth. Sputter rates can be adjusted to analyze depths ranging from nanometres to many microns.

It should now be possible to see if the phaselayer was properly removed and to see if we have an adequate profile. There should be enough boron to avoid etching in the KOH-etch later on. With a content of boron of more than a certain level the beam structures will be masked by the boron. Hopefully it will also be masked to a depth deep enough to ensure the right thickness of the beams.

![Figure 5, SIMS](image)

Depth profiles can be used to: ref.[3]

- Show impurities present in a particular layer, their concentrations, and their depth distributions
- Measure the thickness of a film (by measuring the depth of the SIMS crater using profilometry)
- Monitor a diffusion profile across an interface
- Show whether segregation occurred at an interface
Features of SIMS

- Quantification normally requires reference standards because secondary ion yields are substrate dependent. Well-defined standards of each matrix must be used to calculate an unknown concentration from its signal intensity.
- SIMS is a destructive technique; a crater is formed during the analysis. The rastered area ranges from 0 - 500m.
- The typical analyzed area size is 60m for depth profiles, and 150m for imaging.
- A flat surface is required to obtain the best lateral and depth resolution.
- Samples must be <25 mm in diameter and preferably <5 mm thick.

Primary beam species useful in SIMS include Cs+, O2+, O, Ar+, and Ga+ at energies between 1 and 30 keV. Primary ions are implanted and mix with sample atoms to depths of 1 to 10 nm.

Sputter rates in typical SIMS experiments vary between 0.5 and 5 nm/s. Sputter rates depend on primary beam intensity, sample material, and crystal orientation.

In appendix B, we see the SIMS profiles that have been made. For the 750°C wafer we see that some layer was not removed. This corresponds well to the later results after etching where we see little or no etching. By 800°C the layer seems to have disappeared but this could not be seen after etching, as no etching was observable. At 1000°C the result is the direct opposite as for 800°C. Here we see a layer in the SIMS, but have nice etching when seen under the microscope.

The problems described could be caused by variations between the wafers and insufficient etching of the oxide (step 6) where even very small areas with oxide could ruin the result.

A nice result can be read from the results though. The boron has diffused away from the wafer in the outer 0.1µm. This is interesting when it is compared with the old process where this distance was about 0.2µm. This means that a better surface roughness might be obtainable with this new process at lower temperature.

A profilometer (TENCOR) is used to measure the depth of the crater made by the SIMS to enable the calculation of the proper x-axis for the profile measurements. In the profilometer a small needle with a tip-radius of 5µm runs over the surface.

**Tencor Profilometer**

The Tencor profilometer is used for scanning the surface profile of a wafer. It can measure small vertical features ranging in height from 100 Å to 650µm. The height position of the diamond stylus generates an analogue signal, which is converted into a digital signal stored, analyzed and displayed. The radius of
diamond stylus is 5 microns, and the horizontal resolution is controlled by the scan speed and scans length. There is a horizontal brooding factor, which is a function of stylus radius and of step height. This brooding factor is added to the horizontal dimensions of the steps. The stylus tracking force is set to 50 milligrams. The scanning head contains a viewing camera, a motor driven stylus and analogue electronics to detect and amplify the transducer signal. We used it for studying the surface profiles of our wafers.

**Thickness of craters measured by the profilometer:**

<table>
<thead>
<tr>
<th>Probe nr.</th>
<th>Temperature of drive in. [°C]</th>
<th>Min. thickness [µm]</th>
<th>Max. thickness [µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 outer pos</td>
<td>750</td>
<td>4,746</td>
<td></td>
</tr>
<tr>
<td>3 inner pos</td>
<td>750</td>
<td>5,300</td>
<td></td>
</tr>
<tr>
<td>4 outer pos</td>
<td>800</td>
<td>4,476</td>
<td>4,854</td>
</tr>
<tr>
<td>5 inner pos</td>
<td>800</td>
<td>4,729</td>
<td>4,991</td>
</tr>
</tbody>
</table>

Table 4, Profilometer measurements

**Measurement of resistivity:**

**Four Point Probe**

The four-point probe is used to measure sheet resistance and resistivity of a diffused layer in a silicon substrate, or a deposited conducting film. The system includes a probe head with four probes in a line separated by a distance of 40 mm, a current source and a digital voltmeter (DVM). The current source passes a current, I, through the outer two probes of the probe head, and the voltage drop, V, across the inner two probes is then measured by the DVM. The sheet resistance is proportional to the ratio V/I. There is a multiplication factor (4.53), which depends on the geometry of the probes and the wafer and is used to calculate resistivity of the wafer.

With a four-point probe the bulk resistivity has been measured. Conversion to resistivities is done with the equation:

\[ R_s = \frac{\rho}{t} = \frac{\pi}{\ln 2} \frac{V}{I} = 4.53 \frac{V}{I} [\Omega \text{m}] \]

<table>
<thead>
<tr>
<th>Probe nr.</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature of drive in. [°C]</td>
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<td>800</td>
<td>1000</td>
<td>Old method</td>
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<tr>
<td>Center mes.</td>
<td>1,512</td>
<td>1,074</td>
<td>1,623</td>
<td>0,677</td>
</tr>
<tr>
<td>(R_s[Ωm])</td>
<td>1,638</td>
<td>1,440</td>
<td>1,664</td>
<td>-</td>
</tr>
<tr>
<td>Middle mes.</td>
<td>1,693</td>
<td>1,233</td>
<td>1,640</td>
<td>0,270</td>
</tr>
<tr>
<td>Outer mes.</td>
<td>1,912</td>
<td>1,590</td>
<td>1,640</td>
<td>1,707</td>
</tr>
</tbody>
</table>

Table 5, Resistivity
From these results we see that there is a quite nonuniform resistivity over the wafer surface of up to 50%. As the impurity concentration is inverse proportional to the resistivity some problem has occurred in the process. A possible explanation could be that the boron wafers used for the predoposition were not parallel to the test wafers. This was not possible to avoid and could have some influence. Also the wafers did not have the same placement in the boat making a possible variation.

**Step 8 KOH etch**

Potassium Hydroxide (KOH) etches silicon in the \(<100>\) direction much more rapidly than in other planes. Three different ways were tried. First IPA was used with KOH for etching at 60°C of silicon, followed by a KOH etch without IPA at two different temperatures of 60°C and 80°C.

Three types of etching with KOH are used.

- Etch 1 is 60°C 130 minutes with etch rate 0.3µm/min.
- Etch 2 is 60°C 75 minutes with etch rate 0.45µm/min.
- Etch 3 is 80°C 30 minutes

**KOH etch with IPA**

KOH1, tank1 was used at a temperature of 60°C.

- Measure the density of KOH.
- Calculate the required quantity of IPA and water and add to the tank.
- Dip the wafers in buffer (BHF) for about 30 sec to remove any oxide formed.
- Dip in water for 2 min.
- Rinse in bubbler (water with nitrogen bubbles) for 2 min.
- Put in KOH1 tank1 for 2 hrs 10 min.
- Dip in water and rinse in bubbler for 2 min each.
- Put in ethanol at 70°C for 10 min.

**KOH etch without IPA**

KOH1 tank k2 was used. The procedure was identical to the one stated above and the only difference was absence of IPA and somewhat lower etching times. The etching time of 75 min was used for 60°C and 30 min for 80°C.
Results
The KOH etchings are found to be very different.
The first with IPA tends to make the surface much more smooth then if no IPA is added.
Below this are different enhanced pictures of different sections from the wafers from which you can see the most important characteristics.

750°C

Figure 6, 750°C, etchtype 2

None of the wafers with a boron drive in temperature of 750°C have adequate etching depth. This presumably shows that the phaselayer was not removed.

800°C

Figure 7, 800°C, type 1 etch.
As for 750°C none of the wafers with a boron drive in temperature of 800°C have significant etching depth. This presumably shows that the phaselayer was also not removed at 800°C.

1000°C

By a boron drive in temperature of 1000°C the etch is nice and deep – here seen after the nr. 1 etching.
Again the etching is very nice. On this feature we see the hanging beams but with a very small gap that unfortunately is grown to one part. On the wafer are several different types of gaps and different gap distances.

This is a number 2 etch where the beams are etched almost away.
Diffusion
Diffusion is used to introduce impurities into a substrate usually silicon. Today ion-implantation and rapid thermal annealing mostly replace the diffusion method. Though for cheap mechanical microstructures the method is compatible and under all circumstances worth a discussion for the understanding of distribution of impurities.

In silicon impurity atoms jump through the silicon crystal by interstitial or substitutional diffusion.

The most basic diffusion process in one dimension can be modelled by Ficks first law:

\[ J = -D \frac{\partial N}{\partial x} \]

Where
- \( J \): Particle flux of impurities
- \( D \): Is the diffusion coefficient
- \( N \): Concentration of impurity.

In general we can split the boundary conditions in two, constant source- and limited source diffusion.

**Constant source diffusion**

\[ Q = \int_0^\infty N(x,t) \, dx = 2N_0 \sqrt{Dt} / \pi \]

![Figure 12, Constant source diffusion](image)

See appendix D for SUPREM graphs that show constant source diffusion for two different temperatures.
Limited source diffusion

\[ N(x,t) = \left( \frac{Q}{\sqrt{\pi Dt}} \right) \exp\left(-\frac{x}{2\sqrt{Dt}}\right)^2 \]

Figure 13, Limited source diffusion [Richard C. Jaeger]

The aim of the diffusion modelling is to predict the final profile of the impurities after all processes. In this case the processes consists of:

- Predeposition
- Drive in with oxidation

In the Drive in process the wafers are annealed for 20min. Also in this step a boron-glass layer is formed. This is a very hard layer that has to be eliminated by etching.

To incorporate the phaselayer is a very difficult task that should be computed numerically. In the following section we try this with the commercial programme SUPREM.

From appendix E we see that the depth of the borondiffusion is proportional to \(\sqrt{Dt}\).
Modeling in SUPREM

Description of diffusion model in use
We use the two.dim model in SUPREM stating that full time dependent transient simulation should be performed. The two.dimm model includes interstitial and vacancy movement. This is done by the command:

```
method two.dim grid.oxide=0.005 gridinit.ox=0.005
```

where;
- `grid.oxide` is desired thickness of added gridlayers
- `gridinit.ox` specifies initial oxide spacing

Boron predeposition
Boron predeposition is simulated with the use of the command:

```
diffuse time=107 temp=1125 C.BORON=1.0E20 F.O2=0.2 F.N2=5
```

where;
- `F.O2` is the flow rate of oxygen
- `F.N2` is the flow rate of nitrogen
- `C.BORON` specifies the impurities of ambient gas in atoms/cm\(^3\).

From appendix F it can be seen that whenever oxide is at hand an Xilicon oxide layer is formed. From the same appendix we see that the wet oxidation is much faster than the dry version.

Etching can be simulated with the commands:

```
rate.etch machine=stj_etch1 oxide wet.etch isotropic=0.1 u.m
etch machine=stj_etch1 time=24 minutes dx.mult=0.25
```

where;
- `wet.etch` describes that this is a wet etch
- `time` is etching time
- `isotropic` describes the etching type and speed.

A result of the wet etch simulation shows that the oxide layer will disappear after a certain period.

It was unfortunately not possible to include the phase layer in the diffusive equations. It is however possible to make a profile that matches the experimental data, but this is of little interest since the simulation will not be able to give proper results for the profile after the diffusion. On the other hand many of the characteristics of simple diffusion could be shown.
Conclusion

We have experienced some rather severe problems with the KOH etching when no IPA is added. The wafers look like they are ruined which is almost the case. This might be because of the lowered threshold temperature for selective boron etching. We have measured the roughness of the wafers from type 1 and type 2 etch and found the roughness when no IPA is used is much larger. For the etching the etch type 1 with IPA should be used as the surface will be much nicer.

Some of the difficulties with the SUPREM were not possible for us to overcome. Unfortunately the phaselayer could not be included in the diffusion equations making the simulation rather useless. On the other hand many of the characteristics of simple diffusion could be shown.

In the drive-in process we had quite a few problems with uneven boron deployment on the wafers. This was due to deformed boron nitride wafers so that our test wafers did not have constant space from the boron source. The distance between the silicon and boron nitride wafers was non-uniform because of this deformity.

The SIMS profiles we obtained did not all show the expected results. This could be due to variations from wafer to wafer. An important result was though the ability to improve the boron profile which could possibly minimize the surface roughness of the wafers. This can be seen from appendix B for drive in at 800°C. Another problem is that we did only calibrate the depth axis on the SIMS profiles. This was not a part of this project but would be advisable to do in further investigation.

The best results we obtained with the 1000°C where the phaselayer seems to have disappeared nicely.

Unfortunately the SEM testing was unsuccessful as we could not focus down under the beams. As time was very limited we did not have time to test all wafers and no test specimen from the 1000°C batch was examined, thus no freehanging beam could be seen. It could therefore be nice if the 1000°C wafer with the type 1 etch could be examined in the SEM.

The most important lesson for us has been the daily work in the clean room. This will make the base for us in upcoming work. On the other hand we have learned much more as e.g. that lab work is time-consuming and that theory and practical lab work is distanced quite a lot. To make nice reproducible results with a certain process takes much time and effort. After this 3-week course we have some idea of what goes on in the clean room, so we have an overview of the possibilities and the possible problems.

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References


http://www.eaglabs.com/cai/simstheo/ionsput.htm
## Appendix A  Boron gaps – Process flow

<table>
<thead>
<tr>
<th>Date</th>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
</table>
| 1    | Thermal Oxidation of 600 nm thick SiO₂  
Silicon wafers: n-type, <100>, ρ = 1-20 Ωcm, polished on one side. Box ON66  
Quantity: 10 + 1 for oxide thickness measurement  
RCA clean if necessary  
Boron drive oven: process: wet1000, time (line 45): 2h10min = 130 min (line 45) |  |
| 2    | UV lithography - 1.5 μm resist AZ5214E  
1. HMDS wafers  
2. Resist on front-side, pre-bake on hot-plate. Recepby PR1_5 (includes pre-bake)  
3. Exposure. Positive process  
   Mask “Boron gaps” has marks to alignment to wafer flat.  
   Aligner: KS  
   Exposure time: 16 s was used on 03.05.2002  
   Mode: hard contact  
4. Develop: 45 s was used on 03.05.2002  
5. Hard-bake, in oven, 120°C, 25 min  
6. Asher to strip residual resist in pattern, recipe 19:  
   power: 170 mW  
   O₂: 120 ml, N₂: 20 ml  
   time: 2 min. |  |
| 3    | SiO₂ etch in buffered HF, to define mask for Boron deposition and drive-in  
Etch-rate: 75 nm/min  
Etch time: 8 min |  |
| 4    | Strip resist in acetone and RCA clean |  |
| 5a   | Process A; Boron deposition and drive-in (TL recipe)  
Boron pre-dep oven at 1125°C, program BP1125  
Process time: 01:47 = 107 minutes  
N₂ flow = 5  
O₂ flow = 0.2  
N₂ flow = 3  
O₂ flow = 3  
Beam thickness, when etched in 60°C KOH: y(mm) =3(time/hours)½. |  |
| 5b   | Boron predeposition  
Boron predeposition oven at 1125 °C, program BP1125:  
Process time: 01:47 = 107 minutes  
N₂ flow = 5  
O₂ flow = 0.2  
N₂ flow = 5  
O₂ flow = 0  
Oxidation  
Parameters used 07.05.2002):  
Boron drive-in oven, program WET900  
Process time: (line 45) = 00:30:00  
Anneal time = 00:20:20 |  |
| 6    | Strip oxide in buffered HF  
Use test wafer from step 5 to check etching time  
Etching time  
Process 5a, 27.02.2002: H₂O: 2 min,BHF: 35 min.  
Process 5b, 07.05.2002: H₂O: 2 min, BHF: 24 min. |  |
| 8    | KOH etch  
28% wt KOH + IPA at 60°C  
Etch rate:  
Etch time: 2h 10 min  
Dry in water and alcool |  |

06.06.2002, Anders Kristensen
Appendix B

Boron drive in 750°C taken from the outer part of the test wafer

Boron drive in 750°C taken from the inner part of the test wafer
Boron drive in 800°C taken from the outer part of the testwafer.

Boron drive in 800°C taken from the inner part of the testwafer.
Boron drive in 1000°C, run 1

Boron drive in 1000°C, run 2
Appendix C

go athena

#TITLE: Simple Boron Anneal
#Author: Simon Jespersen, 2002, c971826@student.dtu.dk

#Defining mask
Depo barrier thick=0.1
struck outfile=.history.9
etch barrier start x=-0.1 Y=-20

#the x dimension definition
#line x loc = 0.0  spacing=0.1
#line x loc = 0.1  spacing=0.1

#the vertical definition
#line y loc = 0     spacing = 0.005
#line y loc = 0.5   spacing = 0.02
#line y loc = 4.0   spacing = 0.20

#initialize the mesh
init silicon c.phos=3.0e16 orientation=100

#Set diffusion model
method two.dim grid.oxide=0.005 gridinit.ox=0.005
#method full.cpl cluster.dam high.conc grid.oxide=0.005 gridinit.ox=0.005

#perform uniform boron implant and diffuse
#implant boron dose=2e14 energy=1

#oxidation, Time in min., Temp in C
#diffuse time=107 temperature=1125 weto2
#diffuse time=107 temp=1125 C.BORON=1.0E25 F.O2=0.2 F.N2=5
#diffuse time=107 temp=1125 t.final=700 F.N2=5
#possible cooling? diffuse time=7 temp=1125 t.final=700 C.BORON=1.0E25 F.N2=5

#Oxidation
#diffuse time=30 temp=900 weto2

#extract name="xj" xj silicon mat.occno=1 x.val=0.0 junc.occno=1
#tonyplot

#Strip oxide
#Testmachine, rate in um/min.
#rate.etch machine=stj_etch1 oxide wet.etch isotropic=0.1 u.m
#etch machine=stj_etch1 time=24 minutes dx.mult=0.25

#KOH Etch
#Testmachine, rate in um/min.
#rate.etch machine=stj_etch2 wet.etch isotropic=0.03
#etch machine=stj_etch2 time=130 minutes dx.mult=0.25

#diffuse time=1 temp=800
extract name="xj" xj silicon mat.occno=1 x.val=0.0 junc.occno=1

#plot the final profile

#save the structure
structure outfile=andfex01.str
quit
Appendix D

Diffusion with temperature 500°C

Diffusion with temperature 1000°C
Appendix E

Diffusion with temp 4

Diffusion with temp 16
Appendix F

Wet oxidation for 107min. 1125°C

Oxydation with 1125°C and a flow of O₂: 0.2 std.L/min. and N₂: 5 std.L/min